

In The Claims:

Claims 1-8 (canceled)

Claim 9. (currently amended) A non-volatile memory device, comprising:

a substrate, wherein the substrate has a trench;  
a gate disposed over and completely filling the trench;  
a plurality of spacers located on the sidewalls of the gate;  
a bottom oxide layer disposed between the gate and the trench surface;  
a charge-trapping layer disposed between the gate and the bottom oxide  
layer;  
a top oxide layer disposed between the gate and the charge-trapping layer;  
a plurality of lightly doped regions located in the substrate underneath the  
spacers; and  
a plurality of source/drain regions located at both sides of the trench in the  
substrate.

Claim 10. (original) The non-volatile memory device of claim 9, wherein the gate  
extends over a portion of the substrate outside the trench.

Claim 11. (previously presented) The non-volatile memory device of claim 10,  
wherein bottom oxide layer further extends out of the trench and is disposed between the  
gate and the substrate.

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Claims 12-13 (canceled)

Claim 14. (original) The non-volatile memory device of claim 12, wherein material constituting the spacers comprises silicon nitride.

Claim 15. (original) The non-volatile memory device of claim 9, wherein material constituting the gate comprises polysilicon.

Claim 16. (original) The non-volatile memory device of claim 9, wherein material constituting the charge-trapping layer is selected from the group consisting of a nitride compound, tantalum oxide, titanic strontium and hafnium oxide.

Claim 17. (original) The non-volatile memory device of claim 9, wherein the device further comprises a silicide layer disposed on the gate surface.

Claim 18. (original) The non-volatile memory device of claim 17, wherein material constituting the metal silicide layer is selected from the group consisting of cobalt silicide, titanium silicide, tungsten silicide, molybdenum silicide, platinum silicide and nickel silicide.